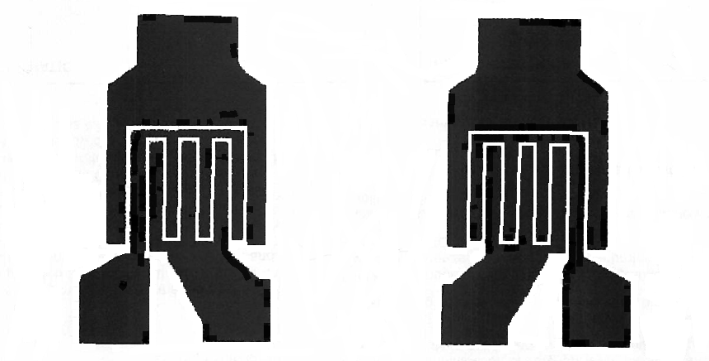
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

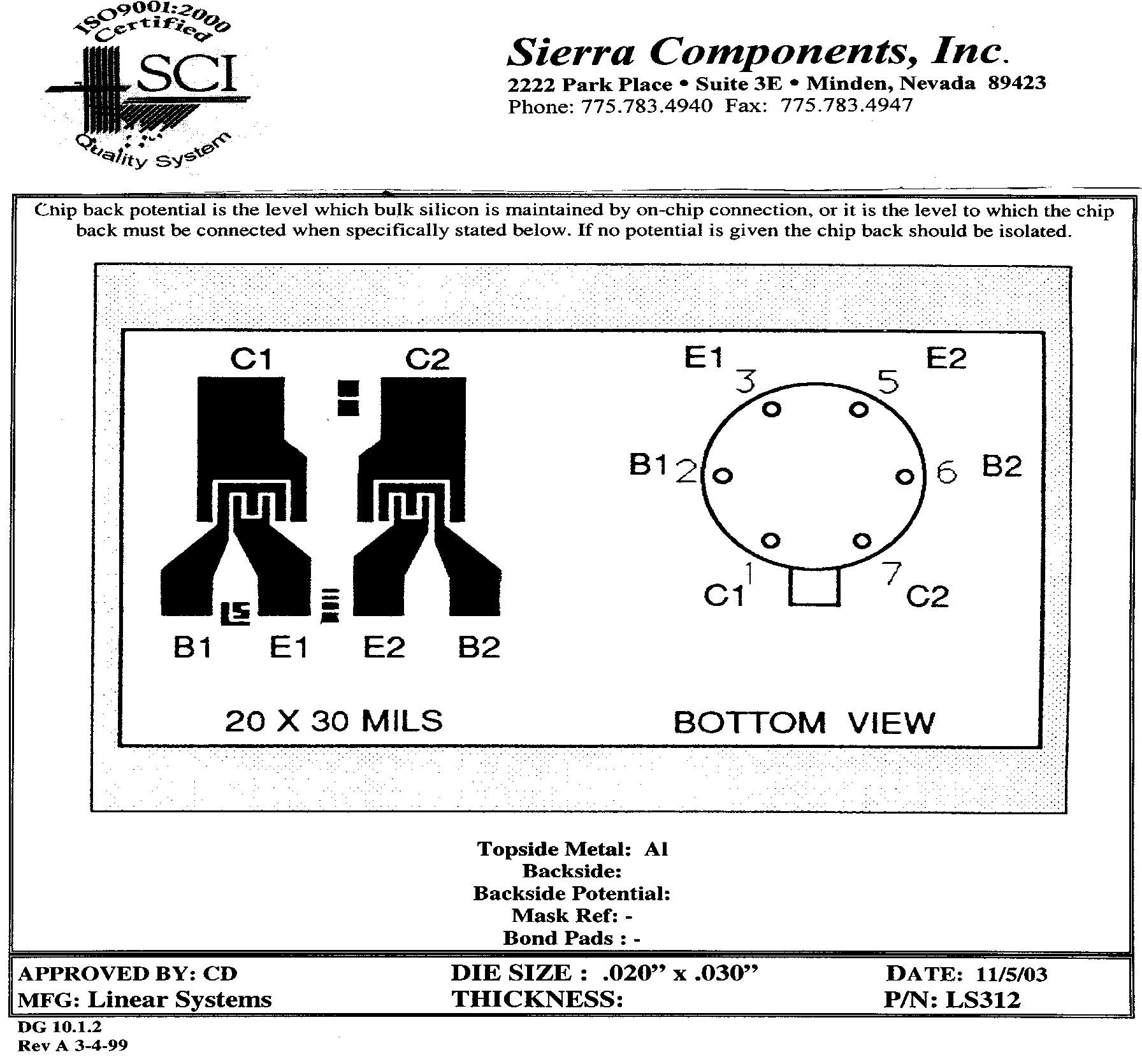
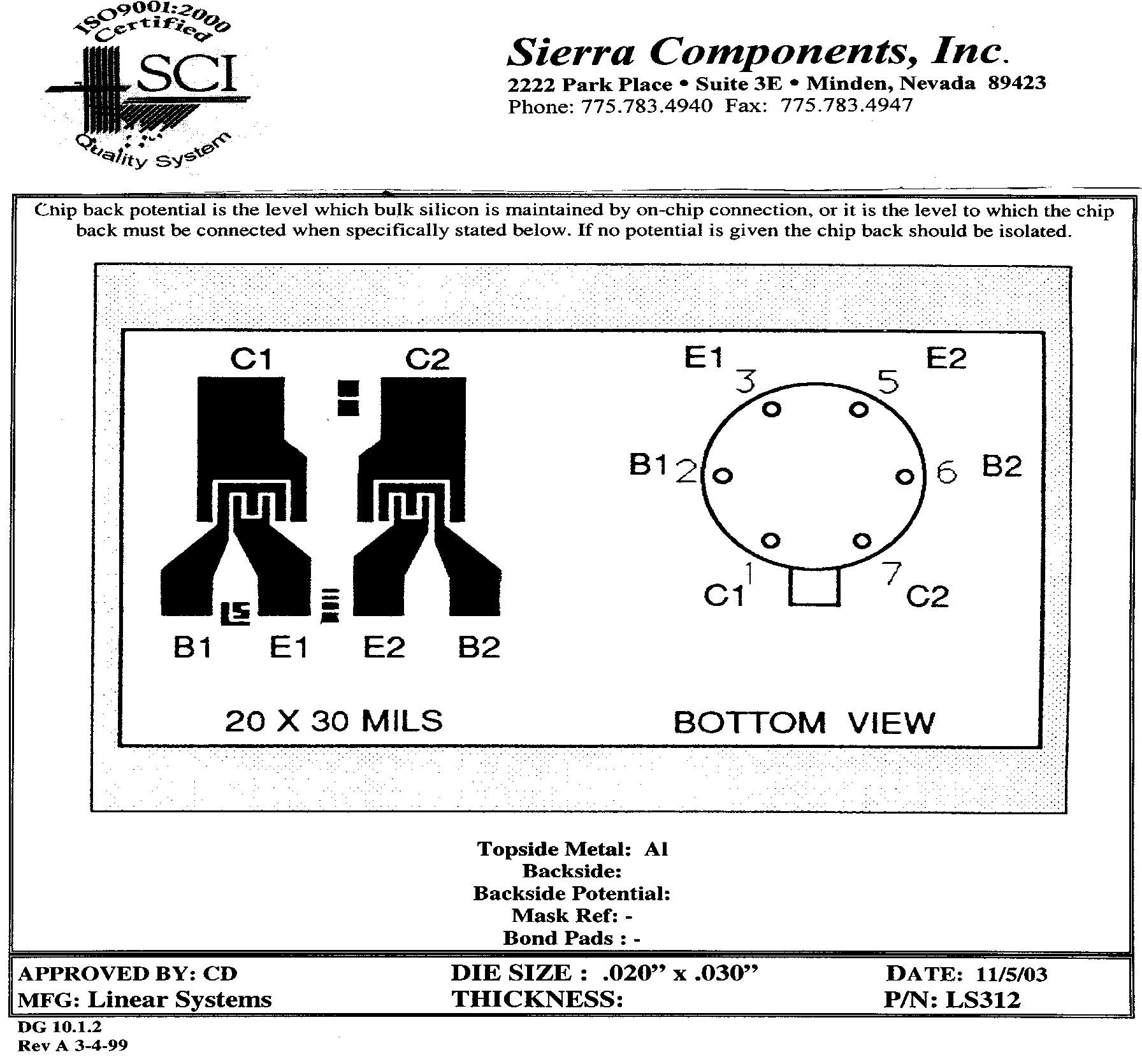


**C C**

**B E E B**

**.023”**

**.038”**

****

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” min.**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .023” X .038” DATE: 3/3/17**

**MFG: LINEAR SYSTEMS THICKNESS .008” P/N: LS3250A**

**DG 10.1.2**

#### Rev B, 7/19/02